

General Description

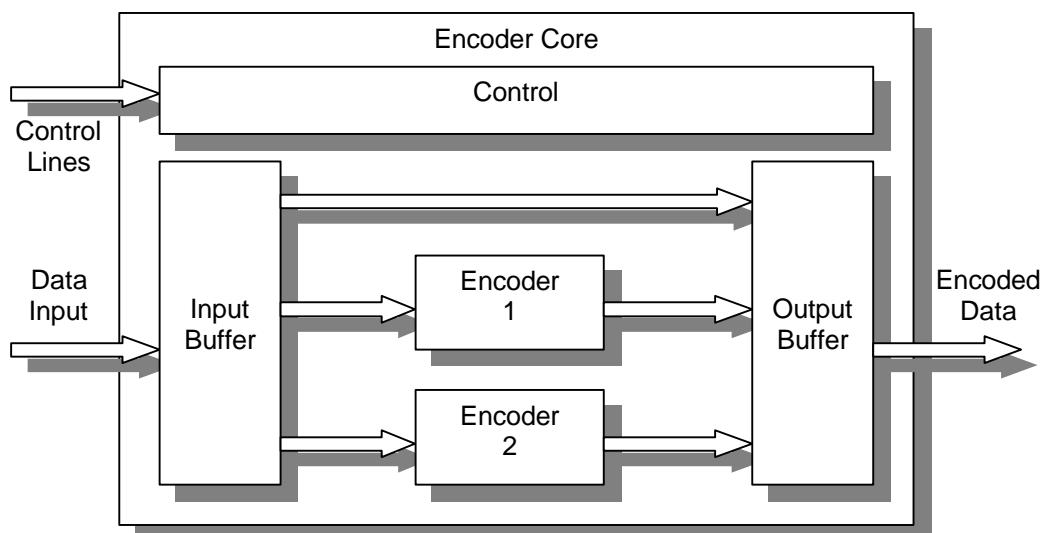
The iCODING DVB-RCS Compliant Turbo Encoder provides a high speed turbo encoder core to partner with the S2000 turbo decoder. The S2001 encoder core provides a simple single data bit input interface and a dual data bit output interface, combined with corresponding framing and valid signals. All programming modes and corresponding pins match those of the S2000 decoder core.

As shown in the block diagram below, a parallel architecture is implemented, using two separate encoder blocks. This architecture has been specifically designed to reduce the encoder processing delay and to provide a very simple yet flexible clock operation.

As the S2001 makes use of valid signals for data input, the encoder can be up-clocked to reduce the encoder processing delay.

Features

- Dropin module for Virtex™-E, Virtex™ -II FPGAs
- No external memory required
- Implements the full DVB-RCS standard encoder for code rates $S \frac{1}{2}$.
- 12 small frame sizes available (96 to 1728 bits), switchable at run-time
- 5 code rates available ($1/2$, $2/3$, $3/4$, $4/5$, $6/7$), switchable at run-time
- Supports data rates up to 95 Mbit/s (Virtex™-II device)
- Low Gate Count
- Asynchronous clocking between data input and output
- Can be up-clocked to decrease encoding delay



Clocking

The S2001 encoder core provides two asynchronous clock inputs; one to clock the data input and drive the encoding process, the other to clock the data out. When operating at a code rate of 1/2, the input and output clocks can be connected directly, resulting in continuous data input and output under normal operation. When operating at higher code rates, the data out clock can be scaled accordingly to provide continuous valid data output, or alternatively a higher clock rate can be used with a data valid out signal employed to signify valid output.

Configuration

The S2001 is primarily available as a Xilinx Virtex[™]-E or Xilinx Virtex[™]-II core. However given the small size of the core, it can be targetted to a variety of FPGAs or ASICs. Please contact iCODING for further information.

For more information on this product, please contact



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