iCODING™ technology incorporated

S2002

DVB-RCS Compliant Turbo Encoder/Decoder

V1.0 17th October 2001 — Product Brief

General Description

The iCODING S2002 DVB-RCS Turbo Codec is one of the world's most advanced FEC codecs. It outperforms many other commercially realizable FEC codes including Block Turbo Codes to give your communications application excellent FEC performance. The convolutional based turbo code typically outperforms block turbo codes by 0.5 to 1.0 dB for most code rates. Performance improvements over the standard K=7 Convolutional code are typically 4dB. Improvements over other FEC techniques varies between 2-5dB.

The S2002 implementation combines the S2001 encoder and S2000 decoder into one core. In addition, a programmable microprocessor interface is provided to allow full programming of both encoder and decoder modes. Note both the encoder and decoder operate completely independently in full duplex operation. The microprocessor interface allows different block sizes up to 256 bytes and different code rate puncturing to be programmed, resulting in a very flexible codec core.

The S2002 implements the DVB-RCS standard, which has been targeted for the return channel (uplink) for a two way satellite data link. However, due to the exceptional flexibility and performance, the S2002 can be used in a wide variety of communications links. Possible applications include; one way satellite communications systems, terrestrial wireless communications systems, and wireline communication systems.

Features

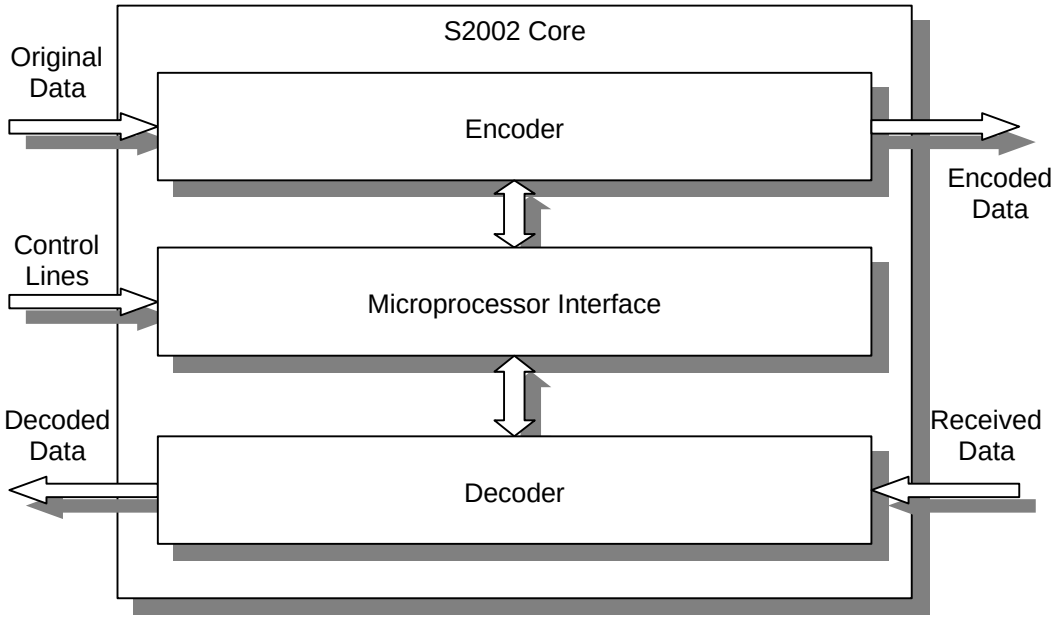
Performance

- Full Duplex DVB-RCS encoder and decoder operation,
- Decoder supports data rates of up to 9 Mbit/sec for 3 iterations in Virtex™-E FPGA,
- Decoder supports data rates of up to 15 Mbit/sec for 3 iterations in Virtex™-II FPGA,
- Decoder supports data rates of up to 45 Mbit/sec for 4 iterations in ASIC,
- Encoder supports data rates up to 95 Mbit/s,
- Achieves QEF performance (BER 10^{-10} and lower) for small frame sizes.

Functionality

- Implements a DVB-RCS compliant turbo encoder and decoder for code rates greater than ½ (ETSI EN 301 790),
- Available as ASIC, Xilinx Virtex™-E or Virtex™-II core,
- Programmable frame sizes from 1 to 256 bytes (8 to 2048 bits),
- 4 switchable frame sizes, switchable on a frame-by-frame basis,
- 5 code rates available (1/2, 2/3, 3/4, 4/5, and 6/7 QPSK), switchable on a frame-by-frame basis,
- Other code rates can be supported by performing puncturing and depuncturing externally,
- Higher order modulation schemes can be supported by inputting LLRs directly,
- Programmable number of decoder iterations
- Flexible clocking, allowing for continuous input and/or continuous output operation,
- Control is switchable between dedicated control pins and microprocessor interface,
- Support for both Intel™ and Motorola™ style microprocessor bus interfaces,
- Built-in 16 bit CRC insertion and detection when packet error detection is required,
- Programmable decoder clock multiplier, using an internal PLL.

iCODING Technology Incorporated
11770 Bernardo Plaza Ct, STE 466
San Diego, CA 92064



Configuration

The S2002 is available as a Xilinx Virtex™-E, Xilinx Virtex™-II or an ASIC core.

For more information on this product, please contact

iCODING technology incorporated

11770 Bernardo Plaza Court, STE 466
San Diego, CA
USA
Phone: +1-858-487-5595
Fax: +1-253-763-8647
E-mail:sales@icoding.com
URL:www.icoding.com