iCODING™ technology incorporated

S2100

DVB-RCT Compliant Turbo Decoder

Version 1.0 - 26th October 2001 Product Brief

General Description

DVB-RCT is currently being developed as a terrestrial return link channel for an interactive service for terrestrial digital television. The turbo code specified for DVB-RCT uses the same turbo code as specified in the DVB-RCS standard but with the following modifications:

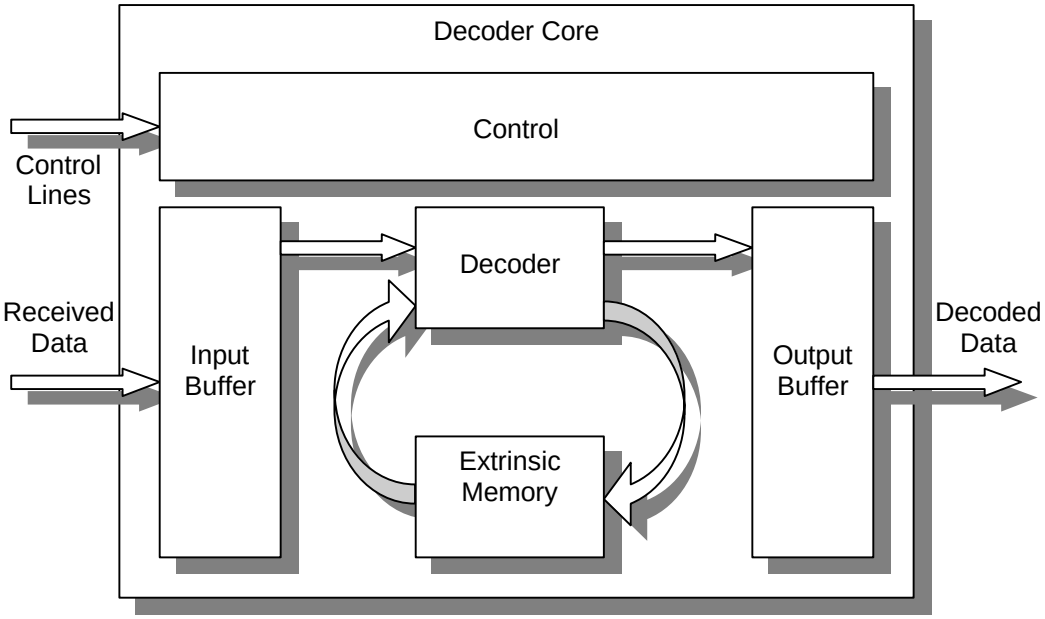
- 3 modulation signal sets supported
- Channel bit interleaver employed
- Reduced number of frame sizes supported
- Reduced number of code rates supported

The iCODING DVB-RCT compliant turbo decoder provides a full implementation of the current DVB-RCT draft standard, including all three modulation signal sets, switchable on a per frame basis and the channel bit interleaver included as part of the decoder core front end.

As DVB-RCT is a multiple access channel, the flow of packets through the decoder will vary in time. As a result, the S2100 is provided with extra control circuitry to handle the asynchronous packet flow.

Features

- Dropin module for Virtex™-E, Virtex™ –II FPGAs
- No external memory required
- Implements the full DVB-RCT standard decoder
- 3 modulation signal sets supported (QPSK, 16QAM, 64QAM), switchable at run-time
- 5 small frame sizes available (144 to 648 bits), switchable at run-time
- 2 code rates available (1/2, 3/4), switchable at run-time
- Includes channel de-interleaver
- Supports data rates up to 31 Mbit/s
- Core area and speed can be tailored for the three carrier spacing modes
- Low Gate Count
- Achieves Quasi-Error Free QEF performance (BER 10^{-10} and lower) for small frame sizes.
- Simple single clock operation



Core Options

The required data throughput of the DVB-RCT system is dependent on a number of initial system and real-time parameters. The most important of these with respect to maximum data throughput are the number of carriers selected (1k or 2k) and the resultant carrier spacings (3 specifications available; CS1, CS2 and CS3). Table 1 provides the maximum data throughputs for each possible setting. Note that these throughputs have been calculated using the operational settings of 64QAM, rate 3/4, rectangular shaping and burst type BS1 or BS2 selected. As the S2100 decoder core is very flexible with respect to speed and area requirements, the core can be configured for a particular speed requirement so the resultant area and memory requirements are minimised.

Table 1 – Data Throughput Requirements

Carrier Spacing	Number of Carriers	Data Throughput Requirement (Mbit/s)
CS1	1k	up to 3.84
CS1	2k	up to 7.68
CS2	1k	up to 7.68
CS2	2k	up to 15.36
CS3	1k	up to 15.36
CS3	2k	up to 30.72

The S2100 is currently available as a Xilinx Virtex-E or Xilinx Virtex-II core, or alternatively it can be customised as an ASIC core.

For more information on this product, please contact

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