iCODING™ technology incorporated

S3000

3GPP (WCDMA) Compliant Turbo Decoder

Version 1.1 – 30th January 2002 Product Brief

General Description

The iCODING S3000 Turbo Decoder implements the standard 3GPP™ universal mobile telecommunications system (UMTS), rate 1/3, 8-state PCCC turbo decoder. It uses a highly efficient architecture to minimise area and memory usage whilst still providing the high performance through the use of a full log MAP implementation, combined with good internal parameter scaling/quantisation. This is all at a data throughput of up to 7 Mbit/s in FPGA. Handset throughputs of 2Mbit/sec are achieved with clock rates as low as 19 MHz.

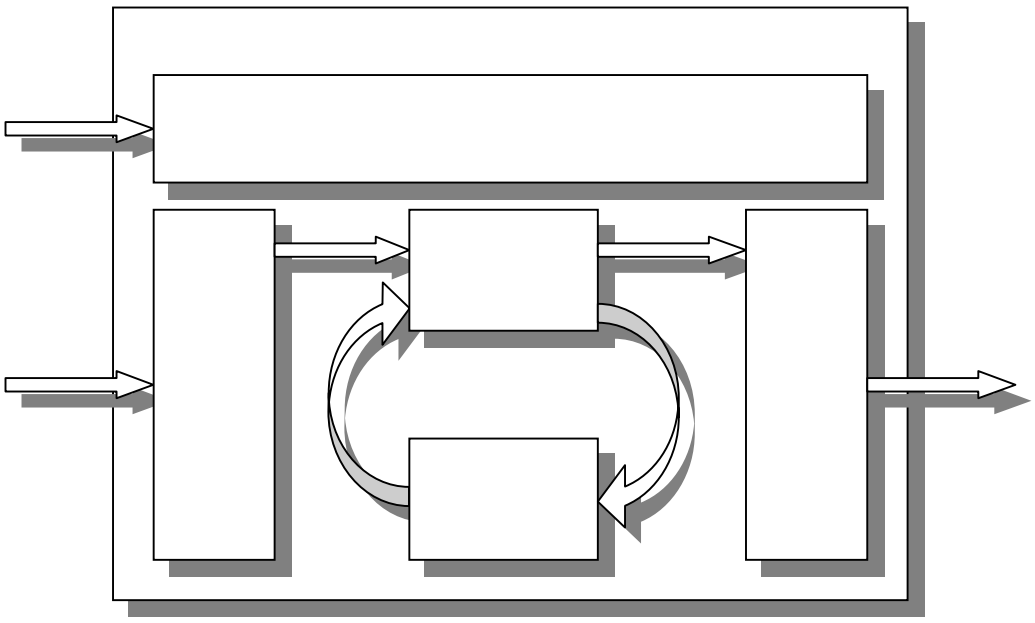
Control of the S3000 is performed via dedicated control pins, with frame settings updated on a per frame basis. Due to the framing signals used, frames can be input in a non-periodic manner if desired.

As with most iCODING products, the S3000 is within the 3GPP specification by varying speed/area/performance tradeoffs or outside it, by varying such parameters as code rates, modulation and block sizes.

Features

General features of the S3000 decoder include:

- Implements the full 3GPP™ standard turbo decoder (3GPP TS 25.212 version 4.1.0 Release 4).
- Drop-in module for Virtex™-E, Virtex™ –II FPGAs
- No external memory required
- Implements a rate 1/3, 8-state PCCC turbo decoder.
- Frame sizes available from 40 to 5114 bits, switchable on a per frame basis
- Programmable number of iterations (1 to 15), switchable on a per frame basis
- Supports data rates of 7 Mbit/s
- Full Log MAP implementation (MAX-log available)
- Low Gate Count
- Simple single clock operation



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Differentiators

The iCODING S3000 Turbo Decoder stands out for the following features:

- Superior BER performance. Various algorithmic improvements provide materially superior performance.
- 100% internally generated interleavers for all frame sizes (40 to 5114). No external calculation or parameter loading.
- Early stopping reduces iterations and power consumption.
- Very low clock-rate-to-data-throughput ratio. 2 Mbit/sec throughput at 8 iterations using 36 MHz clock and at 4.5 iterations using a 19 MHz clock.
- Deliverables include fading channel application note that describes methods for realizing the additional coding gain of the full log-MAP decoder in a real world channel. Gains from using full log-MAP can be combined with early stopping for power savings.
- Automatic disabling of idle external memories.
- Complementary K=9 3GPP compliant Viterbi Decoder available.
- Two interface options: serial interface and external memory interface (addressable).
- As much as half the gate count of other designs. Please contact for FPGA and ASIC gate counts.
- Up to 7 Mbits/sec throughput at 4 iterations with 75 MHz clock for base station support.

Deliverables

- Gate Level Netlist (FPGA)
- Synthesizable RTL Code (ASIC)
- Synthesis scripts (Design Compiler)
- Bit Exact C Libraries. Useful for generating test vectors.
- Test Bench and Vectors
- Complete Documentation
- Application Note
- Gate Level Netlist (FPGA)

Configuration

The S3000 is primarily available as a Xilinx Virtex™-E, Xilinx Virtex™-II and as an ASIC core, but can be synthesized for alternative devices. Please contact iCODING for further information.

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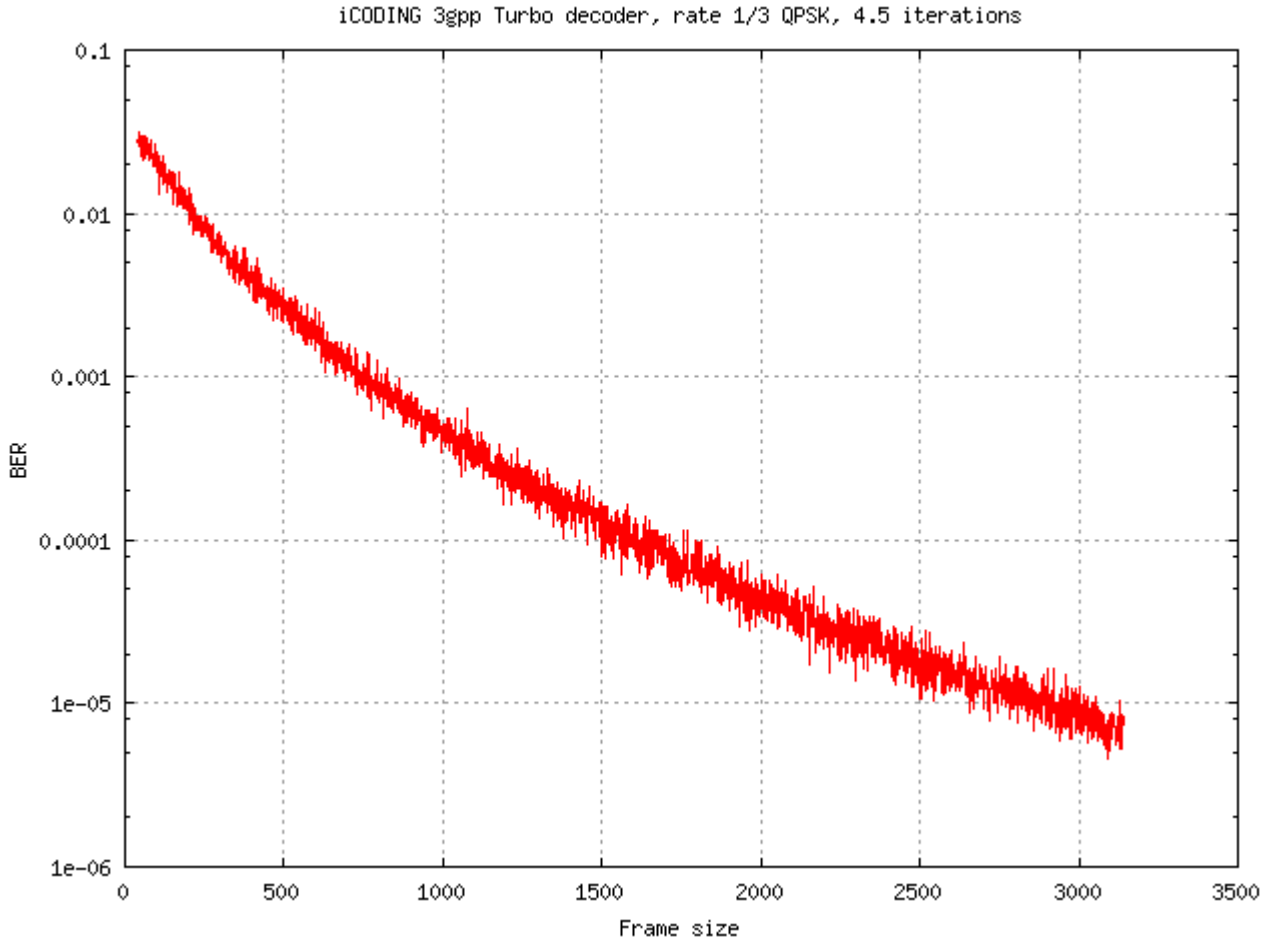

Bit exact (FPGA) BER results for range of frame sizes at 1.0 dB Eb/N0 and 4.5 iterations.

For more information on this product, please contact

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