iCODING™ technology incorporated

S4000

220 Mbit/s High Speed FPGA Turbo Decoder

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General Description

The iCODING S4000 High Speed FPGA Turbo Decoder provides leading technology turbo code performance at exceptional data throughputs. Using the highly parallelizeable iCODING decoding core as a basis, the S4000 can achieve speeds in a single FPGA which were previously only possible in ASIC. Designed for both Virtex™-E and Virtex™ –II Xilinx series of FPGAs, a wide range of speed/performance tradeoffs can be achieved, dependent on the selection of FPGA size and maximum block size.

To help maximise the data throughput for a given FPGA size, two different parallel architectures are available;

- a high latency implementation which operates faster but requires more memory, and
- a low latency implementation which operates slower but requires less memory.

The low latency implementation outputs each decoded frame within the time to input one frame of data, whereas the high latency implementation will exceed this.

When fitting the S4000 to a particular Xilinx FPGA, to maximise the throughput, the design will either be area limited or memory limited. With two architectures available, greater data throughput options are available, allowing the smallest FPGA to be selected for a given set of requirements.

The S4000 is a totally flexible product which can be tailored to the designers needs. Operating variables such as modulation, code rate and frame size selections can all be tailored to a wide variety of communications links. Possible applications including one way satellite communications systems, terrestrial wireless communications systems, and wireline communication systems.

Features

- Data Throughputs of 160 Mbit/s or higher in a single Virtex™-II and 50 Mbit/s or higher for Virtex™-E.
- Latency remains less than 2 times the frame transmission time for all data rates.
- Data rate not affected by change in code rate – same data rates achievable for rates ½ to 6/7.
- Uses convolutional constituent codes for highest error correcting performance
- Drop in module for Virtex™-E, Virtex™ –II FPGAs
- No external memory required
- Achieves QEF performance (BER 10^{-10} and lower) even for small frame sizes.
- Flexible clocking options available, allowing for continuous input and/or continuous output operation
- RTL core available for ASIC for 220 Mbit/sec or higher performance
- 8 state (-88) or 16 state (-FF) constituent codes supported
- C simulation libraries available
- PCI evaluation board available
- Evaluation core available

Flexible Design Allowing

- Frame sizes up to 16384 bits, switchable at run-time if required
- 16 code rates from 1/2 to 16/17 switchable at run-time, if required. Other code rates available upon request.
- Programmable number of decoder iterations
- Various modulation schemes supported including QPSK, 8PSK, 16QAM, 64QAM.

Data Throughput can be tailored by varying

- Degree of parallelization
- Part Selection
- Maximum Frame Size
- Number of Iterations

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Configuration

The S4000 is a highly configurable core which can be tailored to a particular Xilinx Virtex FPGA by selecting the level of parallelization, the maximum frame size and the number of iterations required. As mentioned, the decoder that will fit in a particular FPGA component can be limited by either the number of CLBs required or the number of block RAMs required and is thus not a straight forward calculation. As a result, the following tables have been provided which show typical data throughputs available for Virtex™-E and Virtex™-II series of FPGAs, for maximum frame sizes of 2048, 8192 and 16384. Results have been generated for both low and high latency architectures. Note that the low latency implementation is best suited to the larger block sizes.

Table 1 – Typical Data Rate (Mbit/s) for Virtex™-E components, Block Size = 2048

Part Number	Latency	Iterations					
		1.5	2.0	2.5	3.0	3.5	4.0
XCV400E-8	high	27	20	16	13	11	10
XCV600E-8	high	27	20	16	13	11	10
XCV1000E-8	high	73	55	44	36	31	27
XCV1600E-8	high	97	73	58	48	41	36
XCV2000E-8	high	122	91	73	61	52	45
XCV2600E-8	high	146	110	88	73	62	55
XCV3200E-8	high	195	146	117	97	83	73
XCV400E-8	low	27	20	16	13	11	10
XCV600E-8	low	27	20	16	13	11	10
XCV1000E-8	low	53	40	32	26	23	20
XCV1600E-8	low	63	47	37	31	27	23
XCV2000E-8	low	70	52	42	35	30	26
XCV2600E-8	low	78	58	46	39	33	29
XCV3200E-8	low	85	64	51	42	36	32

Table 2 – Typical Data Rate (Mbit/s) for Virtex™-II components, Block Size = 2048

Part Number	Latency	Iterations					
		1.5	2.0	2.5	3.0	3.5	4.0
XC2V1000-5	high	38	28	22	19	16	14
XC2V1500-5	high	55	41	33	27	23	20
XC2V2000-5	high	83	62	49	41	35	31
XC2V3000-5	high	110	83	66	55	47	41
XC2V4000-5	high	166	124	99	83	71	62
XC2V6000-5	high	266	199	159	133	114	99
XC2V8000-5	high	360	270	216	180	154	135
XC2V10000-5	high	495	371	297	247	212	185
XC2V1000-5	low	38	28	22	19	16	14
XC2V1500-5	low	46	35	28	23	20	17
XC2V2000-5	low	64	48	38	32	27	24
XC2V3000-5	low	71	53	42	35	30	26
XC2V4000-5	low	98	73	58	49	42	36
XC2V6000-5	low	126	94	76	63	54	47
XC2V8000-5	low	138	103	83	69	59	51
XC2V10000-5	low	154	115	92	77	66	57

Table 3 – Typical Data Rate (Mbit/s) for Virtex™-E components, Block Size = 8192

Part Number	Latency	Iterations					
		1.5	2.0	2.5	3.0	3.5	4.0
XCV600E-8	high	31	23	18	15	13	11
XCV1000E-8	high	63	47	37	31	27	23
XCV1600E-8	high	94	71	56	47	40	35
XCV2000E-8	high	126	94	75	63	54	47
XCV2600E-8	high	126	94	75	63	54	47
XCV3200E-8	high	157	118	94	78	67	59
XCV600E-8	low	31	23	18	15	13	11
XCV1000E-8	low	76	57	46	38	32	28
XCV1600E-8	low	97	73	58	48	41	36
XCV2000E-8	low	117	87	70	58	50	43
XCV2600E-8	low	134	100	80	67	57	50
XCV3200E-8	low	165	124	99	82	70	62

Table 4 – Typical Data Rate (Mbit/s) for Virtex™-II components, Block Size = 8192

Part Number	Latency	Iterations					
		1.5	2.0	2.5	3.0	3.5	4.0
XC2V1000-5	high	44	33	26	22	18	16
XC2V1500-5	high	64	48	38	32	27	24
XC2V2000-5	high	96	72	57	48	41	36
XC2V3000-5	high	132	99	79	66	56	49
XC2V4000-5	high	193	144	115	96	82	72
XC2V6000-5	high	309	231	185	154	132	115
XC2V8000-5	high	418	313	251	209	179	156
XC2V10000-5	high	574	430	344	287	246	215
XC2V1000-5	low	44	33	26	22	18	16
XC2V1500-5	low	61	45	36	30	26	22
XC2V2000-5	low	87	65	52	43	37	32
XC2V3000-5	low	119	89	71	59	51	44
XC2V4000-5	low	152	114	91	76	65	57
XC2V6000-5	low	234	175	140	117	100	87
XC2V8000-5	low	278	208	167	139	119	104
XC2V10000-5	low	350	262	210	175	150	131

Table 5 – Typical Data Rate (Mbit/s) for Virtex™-E components, Block Size = 16384

Part Number	Latency	Iterations					
		1.5	2.0	2.5	3.0	3.5	4.0
XCV1000E-8	high	32	24	19	16	13	12
XCV1600E-8	high	32	24	19	16	13	12
XCV2000E-8	high	32	24	19	16	13	12
XCV2600E-8	high	64	48	38	32	27	24
XCV3200E-8	high	64	48	38	32	27	24
XCV1000E-8	low	32	24	19	16	13	12
XCV1600E-8	low	107	80	64	53	46	40
XCV2000E-8	low	131	98	78	65	56	49
XCV2600E-8	low	153	115	92	76	65	57
XCV3200E-8	low	195	146	117	97	83	73

Table 6 – Typical Data Rate (Mbit/s) for Virtex™-II components, Block Size = 16384

Part Number	Latency	Iterations					
		1.5	2.0	2.5	3.0	3.5	4.0
XC2V1000-5	high	45	34	27	22	19	17
XC2V1500-5	high	66	49	39	33	28	24
XC2V2000-5	high	90	68	54	45	38	34
XC2V3000-5	high	136	102	81	68	58	51
XC2V4000-5	high	198	148	119	99	85	74
XC2V6000-5	high	317	238	190	158	136	119
XC2V8000-5	high	363	272	217	181	155	136
XC2V10000-5	high	408	306	245	204	175	153
XC2V1000-5	low	45	34	27	22	19	17
XC2V1500-5	low	64	48	38	33	27	24
XC2V2000-5	low	94	70	56	47	40	35
XC2V3000-5	low	129	96	77	64	55	48
XC2V4000-5	low	174	130	104	87	74	65
XC2V6000-5	low	272	204	163	136	116	102
XC2V8000-5	low	334	251	200	167	143	125
XC2V10000-5	low	443	332	266	221	190	166

Performance

To aid the selection of the best architecture for a given set of requirements, the coding performance of the S4000 turbo decoder is provided in Figure and Figure . Note these performance curves do not represent the full set of coding options, but give some indication of code performance. Lower speeds allow for greater numbers of iterations and therefore materially higher performance. For specific code performance for your application, please contact iCODING. Also, our lower speed S1000 core is available for the most demanding BER performance needs.

Figure shows the performance of the S4000-FF with a block size of 16384 bits at vairious code rates and iterations. Figure 2 shows the performance of the S4000-88 with a block size of 16384 bits and 3.5 iterations for varying code rates. Figure 3 shows the performance of the S4000-88 with a block size of 16384 bits and a code rate of ¾ for varying number of iterations. This figure can be used in conjunction with Table 5 and Table 6 to conduct a area/speed/performance tradeoff.

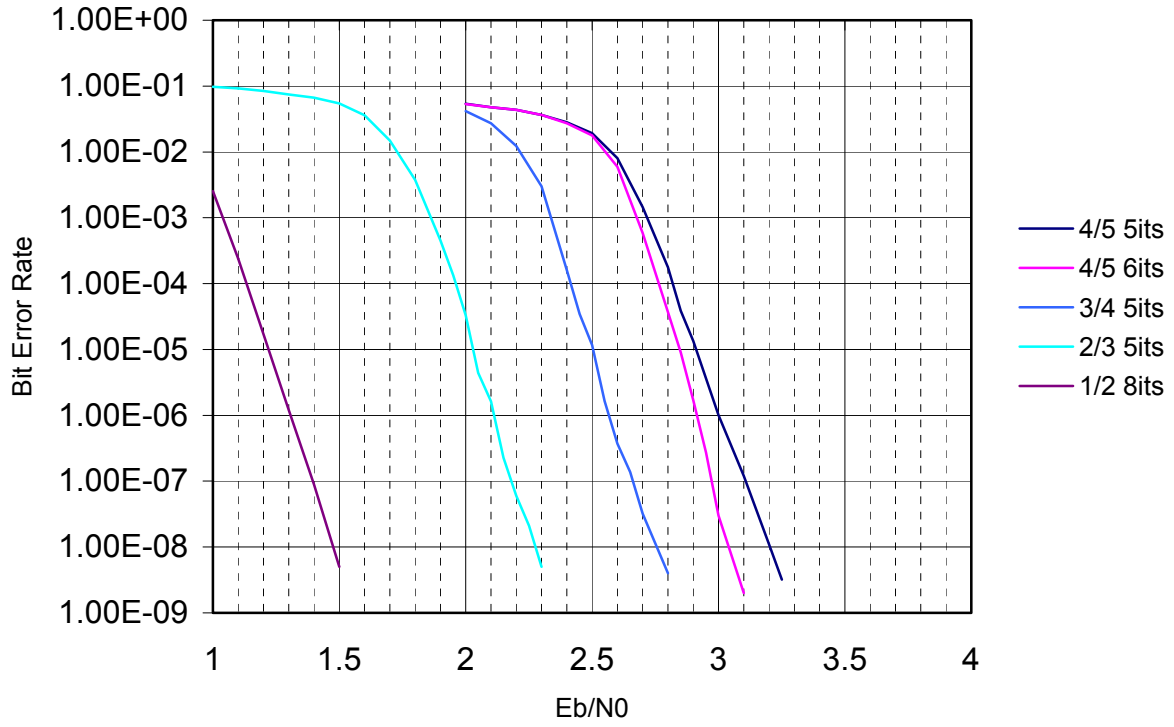

Figure 1 – S4000-FF QPSK, frame size = 16384 bits at various code rates and iterations (its). Results are bit exact and include as much as 0.3 dB implementation loss.

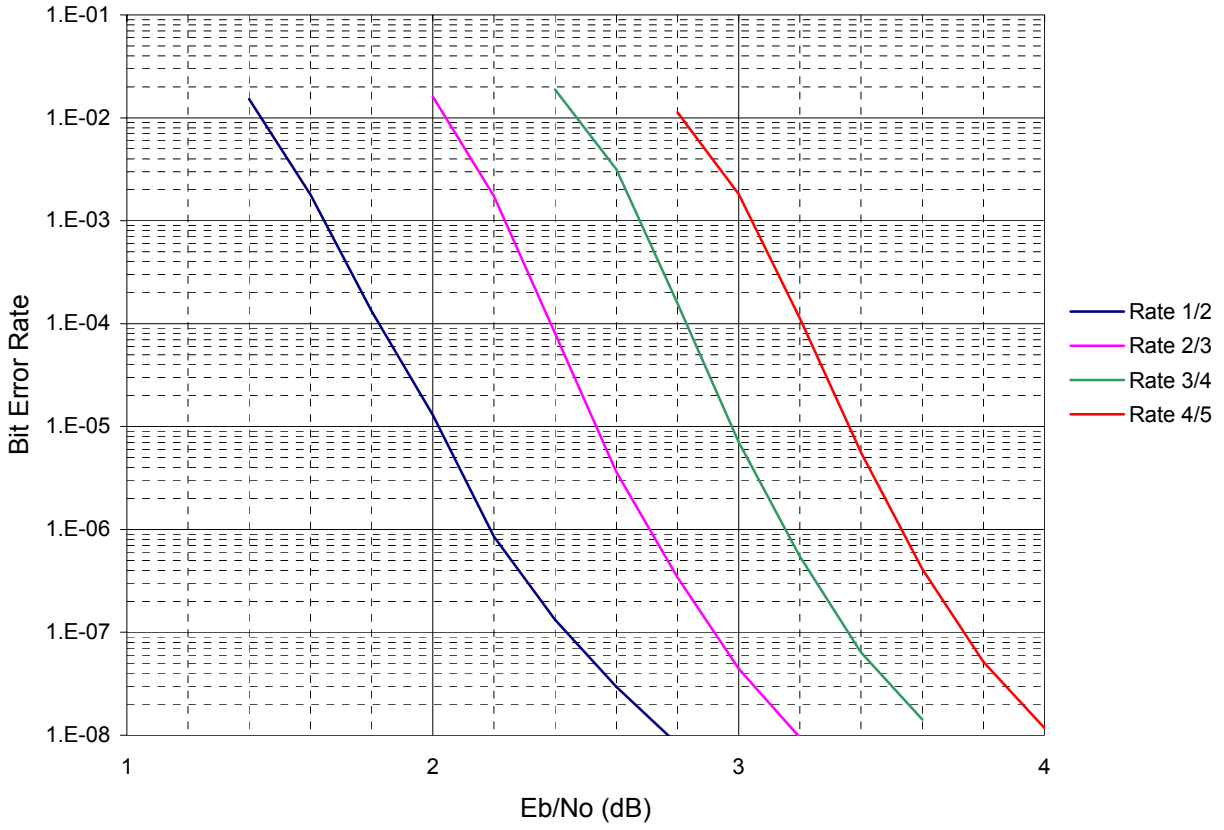

Figure 2 – S4000-88 QPSK, frame size = 16384 bits, 3.5 iterations, BER performance with varying Code Rate

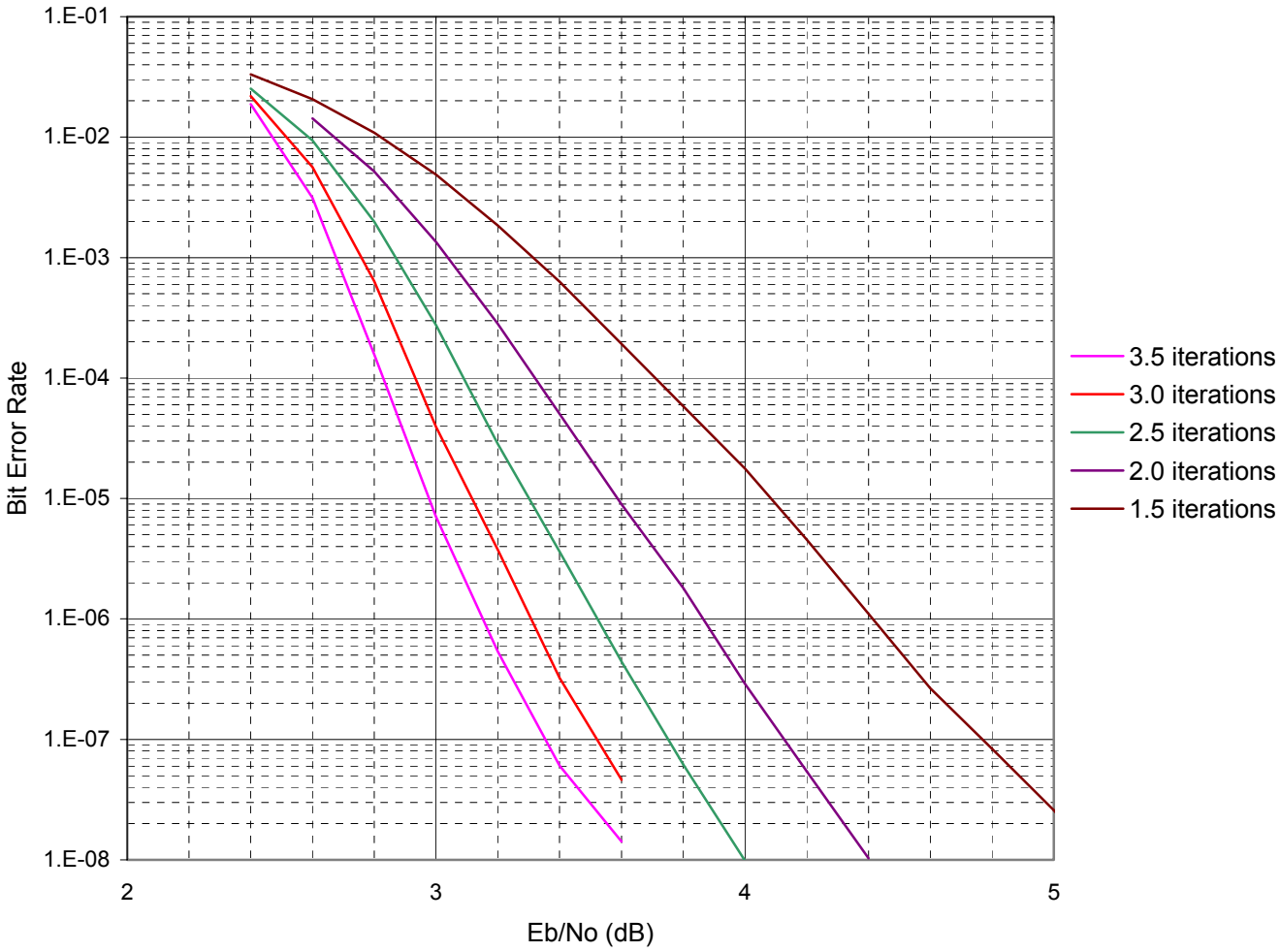

Figure 3 – S4000-88 Rate 3/4 QPSK, frame size = 16384 bits BER Performance with varying number of iterations

Example

Using the maximum data rate tables above, the following table shows an example of the FPGA selection options and resultant BER performance for a Rate 3/4 155 Mbit/s system.

Table 7 – FPGA options for Rate 3/4 155 Mbit/s system

Block Size	Iterations	Latency	Smallest Part	Eb/No @ BER = 1e-7
16384	3.5	high	XC2V8000-5	3.4
16384	3.0	high	XC2V6000-5	3.5
16384	2.5	high	XC2V6000-5	3.8
16384	2.0	high	XC2V6000-5	4.2
16384	1.5	low	XCV3200E-8	4.8

For more information on this product, please contact

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