1 Introduction

The S7000 Turbo Code decoder core is a high speed decoder capable of decoding the 16 state parallel-concatenated convolutional Turbo Code specified by the second-generation DVB-RCS2 standard. The decoder uses multiple parallel MAP decoders to process 4-8 bits per clock cycle with a minimum amount of overhead per iteration.

Figure 1 is a diagram of the Turbo Code encoder that supported by the S7000 Turbo Code decoder.

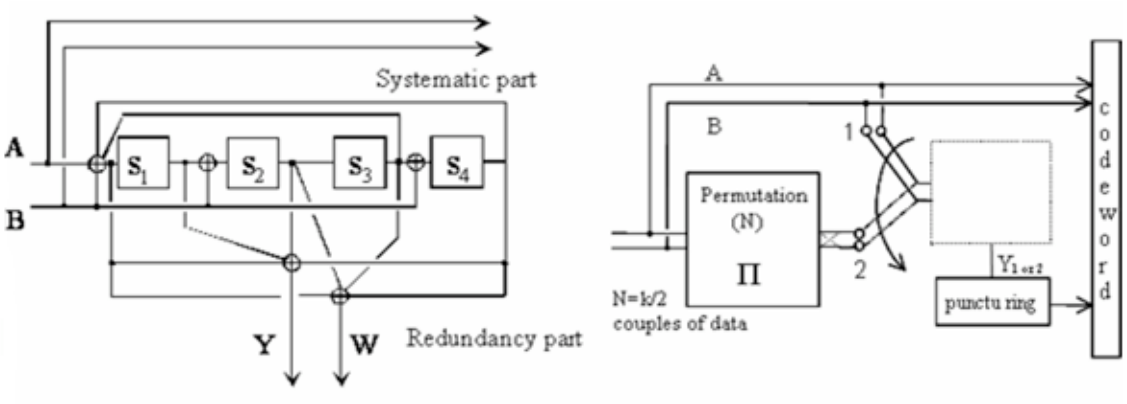

Figure 1. Turbo Code Design

As noted by the diagram K is the number of information bits in the frame and N is the number of di-bits (K/2). Additionally, p refers to the number of parity bits after any puncturing.

The following document describes the basic functionality of the S7000 Turbo Code decoder core. For more detailed information please contact iCODING Technology Inc using the contact information provided below.

2 Options

The S7000 decoder core is customizable in the following areas. Note all options are build-time options unless otherwise specified:

- Bit Widths – The S7000 decoder can be configured for a variety of input sample bit widths. The standard input bit width is 6 bits I/Q samples. Typical input bit widths are between 3-8 bits I/Q samples. Other bit widths can be made available upon request.
- Parallelism – The S7000 is designed to use 2 or 4 map decoders in parallel.

Other customizations are available upon request.

3 Configuration Parameters

A typical configuration for the s7000 Turbo Code decoder core is as follows:

- Inputs are 6 bit received I,Q Symbols
- Supported constellations are QPSK and 8PSK, 16APSK, 16QAM
- Frame sizes: From 12 to 1024 bytes (96 to 8192 bits) when N is not a integer multiple of 15 (Table 1)
- Code Rates: From Rate 1/3 to 0.9, supported rates (Table 2)
- Constellation demapping support (Table 6)

Table 1 – Example Frame Size Support

Frame Size	N	Size in Bytes	Valid
96	42	12	YES
104	46	13	YES
112		14	YES
120	60	15	NO
128		16	YES
136		17	YES
…		…	
224		28	YES
232		29	YES
240		30	NO
248		31	YES
…		…	
8152	4076	1019	YES
8160	4080	1020	NO
8168	4084	1021	YES
8176	4088	1022	YES
8184	4092	1023	YES
8192	4096	1024	YES

Table 2 – Supported Code Rates

Puncture Pattern	Effective Rate
1/3	.333
2/5	.400
1/2	.500
2/3	.666
3/4	.750
4/5	.800
5/6	.833
6/7	.857
7/8	.875
8/9	.888
9/10	.900

Table 3 shows the parity puncturing for the supported code rates.

Table 3 – Code Rate Select Inputs

Code Rate	Y Pattern	W Pattern	Effective Rate
1/3	1	1	0.333
2/5	1	10	0.400
1/2	1	0	0.500
2/3	10	0	0.667
3/4	101000	0	0.750
4/5	1000	0	0.800
5/6	1000 1000 1000 1000 0000	0	0.833
6/7	1000 1000 0000	0	0.857
7/8	1000 1000 0000 1000 0000 1000 0000	0	0.875
8/9	1000 0000	0	0.889
9/10	1000 0000 0	0	0.900

Table 4 shows the control input settings for configuring the input constellation type.

Table 4 – Constellation Selection Inputs

Constellation
BPSK
QPSK
8PSK Option 1
8PSK Option 2
16ASPK
16QAM

4 Clocking

The decoder core uses a single clock for all processing and input and output registering. As the decoder must perform a number of iterations, the input clk must be set to a frequency higher than the data rate. The ratethe rate at which data is input into the decoder may be controlled using a data_valid_in signal. The use of an asynchronous FIFO or other interface may be useful if the data valid signal is not synchronous with the system clock. Additionally, the switching or processing of a previously loaded frame can be suspended by the assertion of a dec_frame_reload signal.

5 Latency

The decoder will automatically start processing once a complete frame has been received. The duration of processing is then dependent on the frame size, the number of null tail bits and the chosen number of iterations. The processing delay (in number of cycles) can be calculated using the following formula:

Delay = (CEILING(FrameSizeBytes/O)*O+1*O+33) * (Num Sub-Iterations) + 2

Where FrameSizeBytes is the frame size in bytes. The factor O is the overlap which is set to 64.

Table 5 provides the throughput calculations for a clock speed of 140 MHz and 16 sub-iterations.

Table 5 – Example Data Throughputs for 140 MHz

Frame Size (Bytes)	Throughput (Mbps)
14	6.1
38	16.5
42	18.2
59	25.6
64	27.8
85	26.4
96	29.9
100	31.1
102	31.7
108	33.6
112	34.8
115	35.8
123	38.2
128	39.8
130	31.5
144	34.9
170	41.2
175	42.4
188	45.5
192	46.5
194	38.5
204	40.4
224	44.4
264	44.3
298	50.0
333	48.4
355	51.6
400	51.4
438	56.2
444	57.0
539	56.1
599	56.9

The throughputs calculated above are provided for example and do not represent an upper limit on the clock rate or throughput of the s7000 core.

For more detailed information about the S7000 Turbo Code decoder core inclduing performance, specific input signals or price and licesing terms please contact iCODING Technology Inc using the contact information listed below.

For more information on this product, please contact

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